

E42 P39Us SPB

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5 ABSTRACT

10 An encapsulated circuit board arrangement comprising a thin interface layer with one or more vias for input/output interface to the circuit. The encapsulated circuit board arrangement further comprises one or more sequentially processed layers added to one side of the interface circuit. The sequentially processed layers are preferably made by additive offset printing technology. The encapsulated circuit board arrangement further comprises a layer of adhesive. A first side of the adhesive layer is attached on top of the uppermost and most exposed layer. The encapsulated circuit board arrangement further  
15 comprises a support carrier attached on a second side of the adhesive layer.

(Fig. 1)